CH32F208 Datasheet

V2.4

Overview

CH32F208 series is an industrial-grade wireless microcontroller designed based on 32-bit ARM® Cortex™-M3 core. The series has a main frequency up to 144MHz and independent GPIO voltage (separate from system power supply). The CH32F208 series has a 12-bit ADC, 2 op-amp comparators, 4 timers and a 32-bit general-purpose timer, and standard communication interfaces such as USART, I²C, SPI, etc. On-chip integration of 2Mbps low-power Bluetooth BLE communication module, 10M Ethernet MAC + PHY module, USB2.0 full-speed device + host / device interface, CAN controller, etc.

Features

- Core:
  - 32-bit ARM Cortex-M3 core
  - Single-cycle multiplication, hardware division, hardware FPU
  - Interruption technology, Fault handling mechanism
  - System main frequency 144MHz
- Memory:
  - Available with up to 64KB volatile data storage area SRAM
  - Available with 480KB program memory CodeFlash (zero-wait application area + non-zero-wait data area)
  - 28KB BootLoader
  - 128B non-volatile system configuration memory
  - 128B user-defined memory
- Power management and low-power consumption:
  - System power supply V_{DD}: 3.3V
  - Independent power supply for GPIO unit $V_{I/O}$: 3.3V
  - Low-power mode: Sleep, Stop, Standby
  - V_{BAT} independently powers RTC and backup register
- Clock & Reset
  - Built-in factory-trimmed 8MHz RC oscillator
  - Built-in 40 KHz RC oscillator
  - Built-in PLL, optional CPU clock up to 144MHz
  - High-speed external 32MHz oscillator
  - Low-speed external 32.768 KHz oscillator
  - Power on/down reset, programmable voltage detector
- Real-time clock (RTC): 32-bit independent RTC timer
- 1 groups of 8-channel general-purpose DMA controllers
  - 8 channels, support ring buffer
  - Support TIMx/ADC /USART/I²C/SPI
- 2 groups of OPAs and comparators: connected with ADC and TIMx
- 1 group of 12-bit ADC
  - Analog input range: V_{SSA}~V_{DDA}
  - 16 external signals + 2 internal signals
  - On-chip temperature sensor
  - Dual ADC conversion mode
- 16-channels Touch-Key detection Timers
- Multiple Timers
  - 1 16-bit advanced-control timers, with dead zone control and emergency brake; can offer PWM complementary output for motor control
  - 3 16-bit general-purpose timers, provide input capture/output comparison/PWM/pulse counting/incremental encoder input
  - 1 32-bit general-purpose timer
  - 2 watchdog timers (independent watchdog and window watchdog)
  - SysTick: 64-bit self-subtracting counter
- Communication interfaces:
  - 4 USART interfaces (including 5 UARTs)
  - 2 I²C interfaces (support SMBus/PMBus)
  - 2 SPI interfaces
  - USB2.0 full-speed device interface

(full-speed and low-speed)
- USB2.0 full-speed host/device interface
- 1 CAN interfaces (2.0B active)
- Low-power Bluetooth BLE5.3

- Fast GPIO port
- 53 I/O ports, with 16 external interrupts
- Security features: CRC unit, 96-bit unique ID
- Debug mode: serial 2-wire debug interface
- Package: LQFP or QFN

Chapter 1 Series product description

The CH32F series are industrial-grade general-purpose enhanced MCUs based on the high performance ARM® Cortex™-M3 32-bit RISC core, which are divided into general-purpose, connectivity, wireless and other categories according to functional resources. They extend each other in terms of package types, peripheral resources and quantities, pin numbers, and device characteristics, but they are compatible with each other in software, functions, and hardware pin configurations. The product iterations and rapid applications provide freedom and convenience for users in product development.

For the features of this series of products, please refer to the datasheet.

For the peripheral function description, usage and register configuration, please refer to "CH32FV2_V3RM".

The datasheet and reference manuals can be downloaded on the official website of WCH:http://www.wch.cn/

For information about the Cortex™-M3 core, please refer to "Cortex-M3 Technical Reference Manual", available for download from ARM website.

This manual is for CH32F208 series datasheet. Please refer to "CH32F203DS0" for F203 series and "CH32V207DS0" for F205, F207 and F203 (high capacity) series.

Table 1-1 Series overview

Low-and-medium capacity general-purpose device (F203)		High capacity general-purpose device (F203)		Connectivity device (F205)	Interconnectivity device (F207)	Wireless device (F208)
32K Flash	64K Flash	128K Flash	256K Flash	128K Flash	256K Flash	128K Flash
10K SRAM	20K SRAM	32K SRAM	64K SRAM	32K SRAM	64K SRAM	64K SRAM
2*ADC(TKey) ADTM 2*GPTM 2*USART SPI I^2C USBD USBFS CAN RTC 2*WDG 2*OPA	2*ADC(TKey) ADTM 3*GPTM 4*USART 2*SPI 2*I^2C USBD USBFS CAN RTC 2*WDG 2*OPA	2*ADC(TKey) 2*DAC ADTM 3*GPTM 3*USART 2*SPI 2*I^2C USBD CAN RTC 2*WDG	2*ADC(TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM 8*USART/UART 3*SPI(2*I^2S) 2*I^2C USBD CAN RTC 2*WDG 4*OPA RNG SDIO FSMC	2*ADC(TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM 5*USART/UART 3*SPI(2*I^2S) 2*I^2C OTG_FS USBHS(+PHY) 2*CAN RTC 2*WDG 4*OPA RNG SDIO	2*ADC(TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM 8*USART/UART 3*SPI(2*I^2S) 2*I^2C OTG_FS USBHS(+PHY) 2*CAN RTC 2*WDG 4*OPA RNG SDIO FSMC DVP ETH-1000MAC 10M-PHY	ADC(TKey) ADTM 3*GPTM GPTM(32) 4*USART/UART 2*SPI 2*I^2C USBD USBFS CAN RTC 2*WDG 2*OPA ETH-10M(+PHY) BLE5.3

Note: The number of peripherals or functions of some products in the same category may be limited by the package, please confirm the product package when selecting.

Abbreviations:

ADTM: Advanced-control Timer

GPTM: General-purpose Timer

GPTM (32):32-bit General-purpose Timer

BCTM: Basic Timer

TKey: Touch key

OPA: Operational Amplifier/Comparator

RNG: Random Number Generator

USBD: Universal Serial Bus Full-speed Device

USBFS: Universal Serial Bus Full-speed Host/Device

USBHS: Universal Serial Bus High-speed Host/Device

Chapter 2 Specification

The CH32F208 series uses the high-performance ARM® Cortex™-M3 32-bit RISC core with a maximum operating frequency of 144MHz, built-in high-speed memory, and multiple buses working synchronously in the system structure, providing a rich set of peripheral functions and enhanced I/O ports. This series has a built-in 12-bit ADC module, multiple timers, multi-channel touch key capacitance detection (TKey), etc. It also contains standard and dedicated communication interfaces: I^2C, SPI, USART, CAN controller, USB2.0 full-speed host/device controller, USB2.0 full-speed device controller, low-power Bluetooth, etc.

The rated working voltage of the product is 3.3V, and the working temperature range is -40°C～85°C in industrial grade. It supports several power-saving operating modes to meet the product's low-power application requirements. Various models in the series are different in terms of resource allocation, number of peripherals, peripheral functions, etc., and can be selected as needed.

2.1 Model comparison

Table 2-1 CH32F208 wireless products resource allocation

Resource Differences \ Product Model			CH32F208 RBT6	CH32F208 WBU6
Pin count			64	68
Flash (bytes) (1)			128K(2)	128K(2)
SRAM (bytes)			64K(2)	64K(2)
GPIO port count			49	53
GPIO power supply			Shared with V_{DD}	Independent power supply $V_{I/O}$
Timer	Advanced-control (16-bit)		1	1
	General-purpose (16-bit)		3	3
	General-purpose (32-bit)		1	1
	Watchdog		2	2
	SysTick (24-bit)		support	
RTC			support	
ADC/TKey (channel@ unit count)			16@1	16@1
OPA			2	2
Communication interfaces	USART/UART		4	4
	SPI		2	2
	I^2C		2	2
	CAN		1	1
	USB(FS)	USBD	1	
		USBHD	1	
	Ethernet		10M	

	BLE5.3	support	
CPU clock speed		Max：144MHz	
Rated voltage		3.3V	
Operating temperature		Industrial-grade: -40°C~85°C	
Package		LQFP64M	QFN68

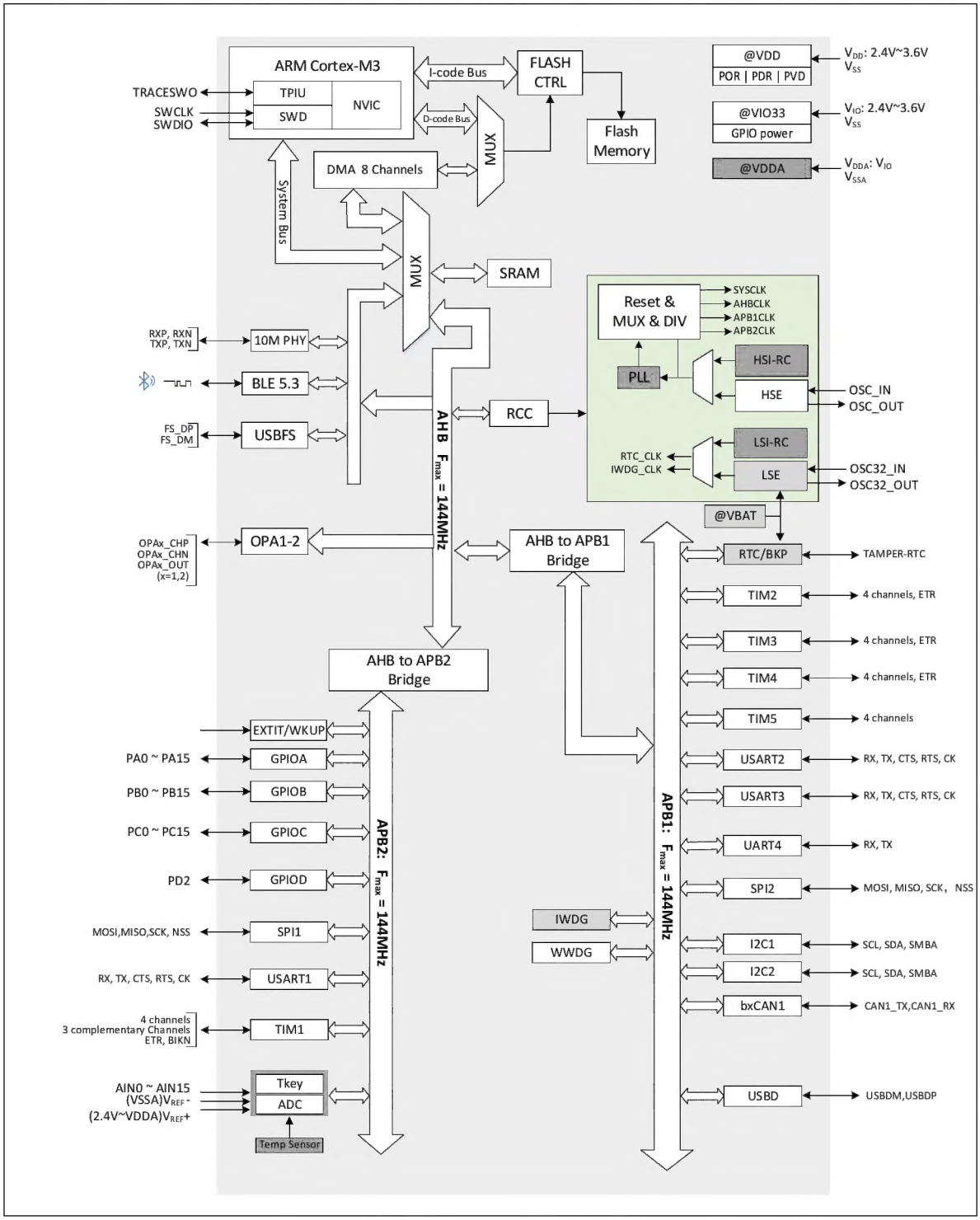
Note: 1. Flash bytes represent zero-wait run area R_{0WAIT}. For the V208 series, non-zero-wait area is (480K-R_{0WAIT}).

2. 128K FLASH+64K SRAM of the 208 product supports user-selected word configuration as one of several combinations of (128K FLASH+64K SRAM), (144K FLASH+48K SRAM), (160K FLASH+32K SRAM).

2.2 System architecture

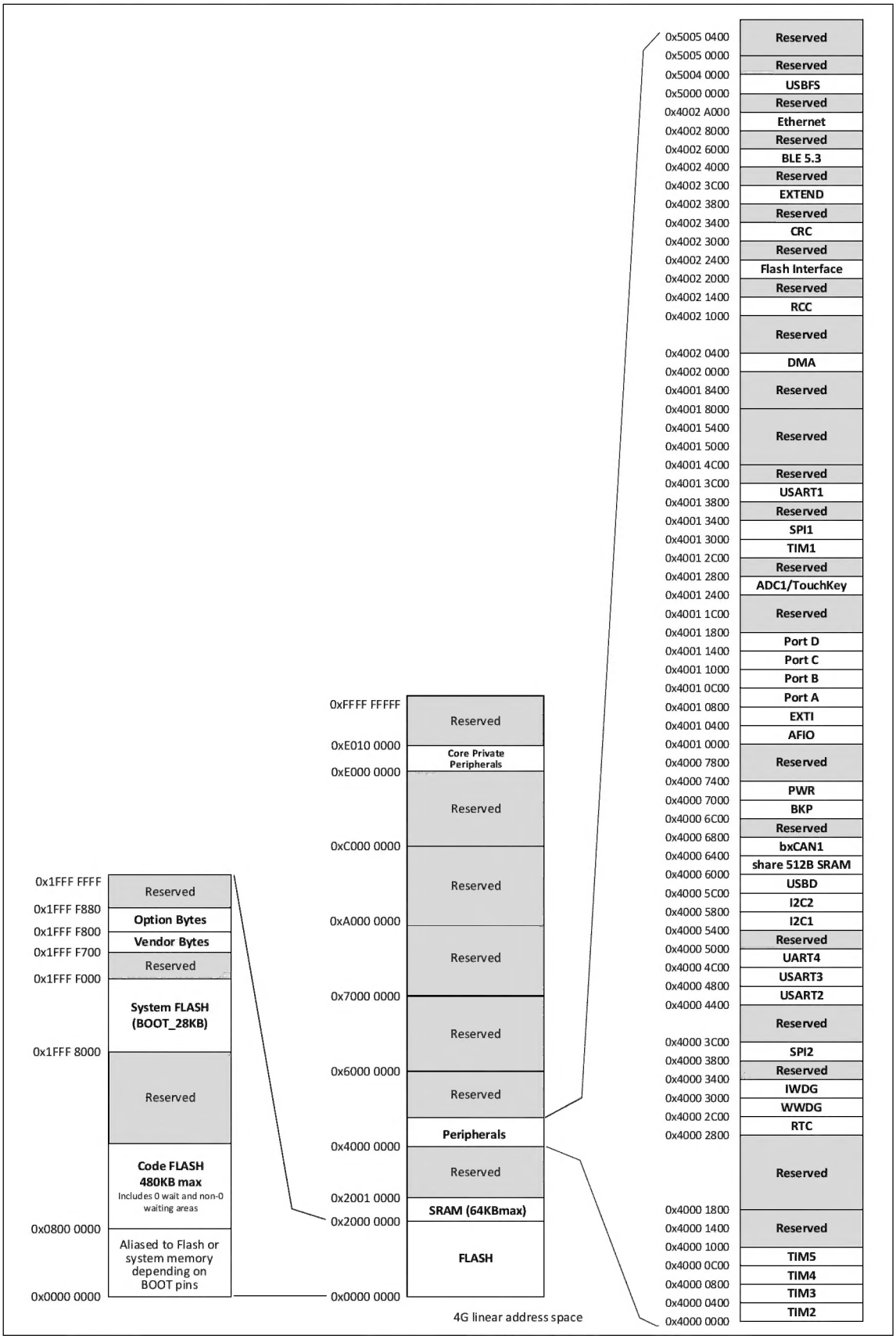
The microcontroller is designed with ARM® Cortex™-M3 as the design core, the architecture of the core, arbitration unit, DMA module, SRAM memory and other parts of the interaction through multiple bus groups. The design integrates a general-purpose DMA controller to reduce the CPU burden and improve access efficiency, and applies a multi-level clock management mechanism to reduce the power consumption of peripherals, as well as a data protection mechanism and automatic clock switching protection to increase system stability. The following figure shows the overall internal architecture of the series.

Figure 2-1 System block diagram



2.3 Memory map

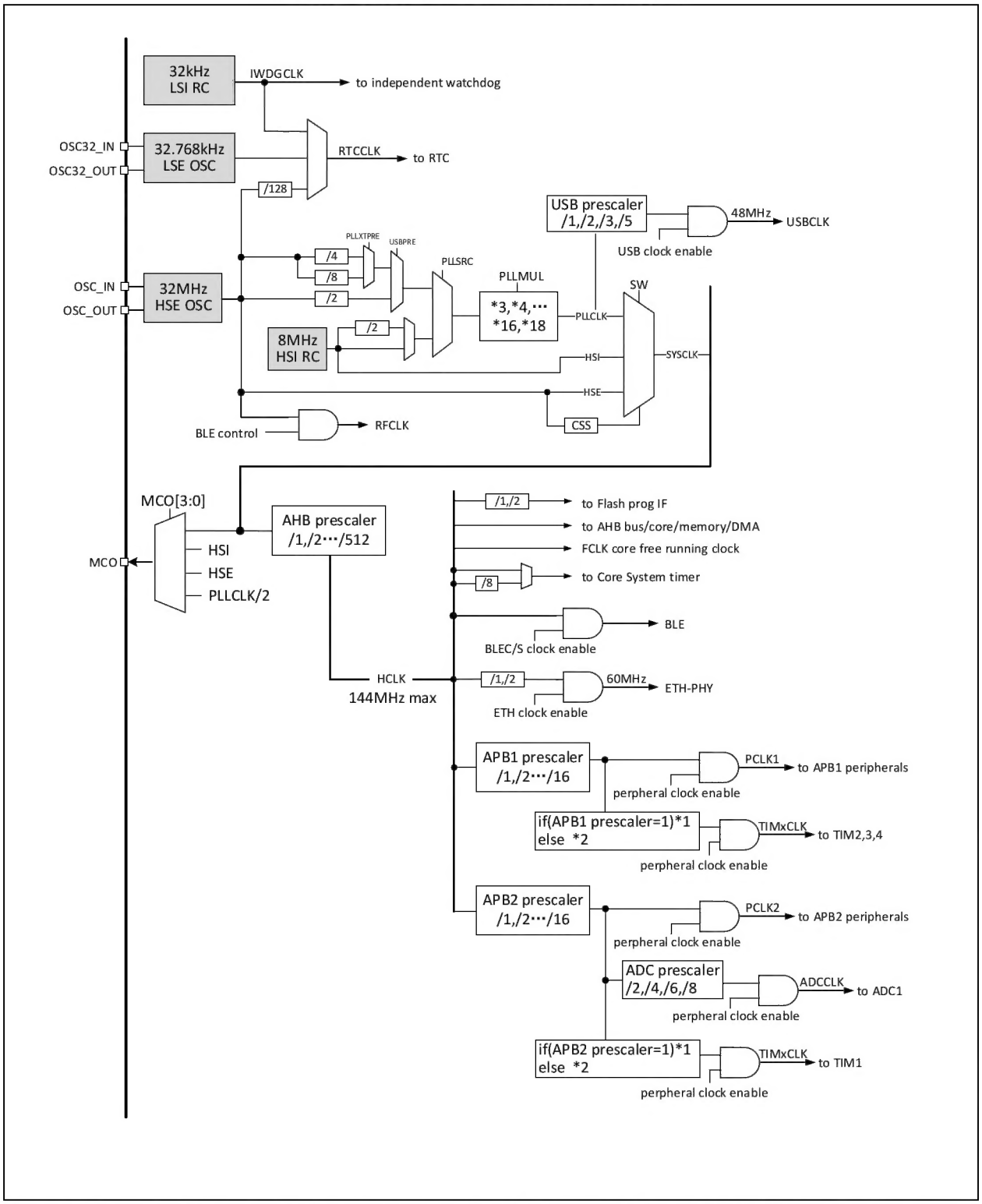
Figure 2-2 Memory address map



2.4 Clock tree

Four groups of clock sources are introduced into the system: internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI), external high-frequency oscillator (HSE), and external low-frequency oscillator (LSE). Among them, the low-frequency clock source provides the clock reference for RTC and independent watchdog. The high-frequency clock source is directly or indirectly multiplied by the PLL and output as the system clock (SYSCLK). The system clock is then provided by each prescaler to provide the AHB domain, APB1 domain, APB2 domain peripheral control clock and sampling or output clock. Some modules need to be directly provided by the PLL clock.

Figure 2-3 CH32F208 clock tree block diagram



Note: 1. When using USB, the CPU clock speed must be 48MHz or 96MHz or 144MHz. When the system wakes up from Stop mode or Standby mode, the system will automatically select HSI as the system clock frequency. If USB and ETH both are enabled, select USBPRE=5DIV, configure PLLCKR=SYSCLK to be 240M, AHBPRE=2DIV, and the CPU clock speed is 120M.

2. For the CH32F208, the external crystal or clock (HSE) is 32M. When the external crystal is enabled, no load capacitor is needed as it is built in.

2.5 Functional description

2.5.1 ARM Cortex-M3 Core

ARM® Cortex™-M3 is a 32-bit embedded processor that provides the low-cost platform, reduced pin count, and reduced system power needed to implement an MCU, as well as superior computational performance and advanced interrupt system response. Its additional code efficiency leverages the high performance of the ARM core on the storage space of typical 8-and 16-bit systems.

- Harvard architecture, add branch prediction function, improve pipeline processor performance play
- Tail-Chaining is a hardware-based technology that improves efficiency
- Core low-power 3 modes, more effective power control
- Advanced Fault handling mechanism, debugging solutions, etc.

The CH32F2x series controllers have a built-in ARM core and are therefore compatible with most ARM tools and software.

2.5.2 On-chip memory and boot mode

Built-in maximum 64K bytes SRAM area for data storage, data loss after power down. The specific capacity should correspond to the chip model.

The built-in program flash memory storage area (Code FLASH) of up to 480K bytes is used for user's application and constant data storage. This includes a zero-wait program run area and a non-zero-wait area. The specific size of the area corresponds to the chip model.

Built-in 28K bytes of system storage (System FLASH) for system bootloader storage (factory-cured bootloader)

128 bytes are used for system non-volatile configuration word storage, and 128 bytes are used for user selection word storage.

At startup, one of 3 boot modes can be selected through the boot pins (BOOT0 and BOOT1):

- Boot from program flash
- Boot from system memory
- Boot from internal SRAM

The bootloader is stored in the system memory, and the contents of the program Flash memory storage can be reprogrammed through the USART1 and USB interface.

2.5.3 Power supply scheme

- V_{DD} = 2.4～3.6V: Power supply for some I/O pins and internal voltage regulator.
- V_{IO} = 2.4～3.6V: It supplies power to most of the I/O pins and the Ethernet module, which determines the pin output high voltage amplitude. Normal work during operation, the $V_{I/O}$ voltage cannot be higher than the V_{DD} voltage.
- V_{DDA} = 2.4～3.6V: It supplies power to the analog part of the high-frequency RC oscillator, ADC, temperature sensor, DAC and PLL. The V_{DDA} voltage must be the same as the $V_{I/O}$ voltage (If V_{DD} is powered down and $V_{I/O}$ is powered on, Then V_{DDA} must be powered on and consistent with $V_{I/O}$). When using ADC, V_{DDA} must not be less than 2.4V.
- V_{BAT} = 1.8～3.6V: When V_{DD} is turned off, (through the internal power switch) independently powers the RTC, external low-frequency oscillator and backup registers. (Pay attention to V_{BAT} power supply)

2.5.4 Power supply monitor

This product integrates a power-on reset (POR)/power-down reset (PDR) circuit, which is always in working

condition to ensure that the system is in supply. It works when the power exceeds 2.4V; when V_{DD} is lower than the set threshold ($V_{POR/PDR}$), the device is placed in the reset state without using an external reset circuit.

In addition, the system is equipped with a programmable voltage monitor (PVD), which needs to be turned on by software to compare the voltage of V_{DD} power supply with the set threshold V_{PVD}.Turn on the corresponding edge interrupt of PVD, and you can receive interrupt notification when V_{DD} drops to the PVD threshold or rises to the PVD threshold. Refer to Chapter 4 for the values of $V_{POR/PDR}$ and V_{PVD}.

2.5.5 Voltage regulator

After reset, the regulator is automatically turned on, and there are 3 operation modes according to the application mode.

- ON mode: Normal operation, providing stable core power.
- Low-power mode: When the CPU enters Stop mode, the regulator can be selected to run with low-power consumption.
- OFF mode: When the CPU enters Standby mode, it automatically switches the regulator to this mode, the voltage regulator output is in high impedance, and the core power.

The voltage regulator is always ON after reset. It is OFF in Standby mode, and the regulator output is in high impedance.

2.5.6 Low-power mode

The system supports 3 low-power modes, which can be selected for low-power consumption, short start-up time and multiple wake-up events to achieve the best balance.

- Sleep mode

In Sleep mode, only the CPU clock is stopped, but all peripheral clocks are powered normally and the peripherals are in a working state. This mode is the shallowest low-power mode, but it is the fastest mode to wake up the system.
Exit condition: any interrupt or wake-up event.

- Stop mode

In this mode, the FLASH enters low-power mode, and the PLL, HSI RC oscillator and HSE crystal oscillator are turned off. In the case of keeping the contents of SRAM and registers not lost, the Stop mode can achieve the lowest power consumption.
Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, among which EXTI signal includes one of 16 external I/O ports, PVD output, RTC alarm clock, Ethernet wake-up signal or USB wake-up signal.

- Standby mode

In this mode, the main LDO of the system is turned off, the low-power LDO supplies power to the wake-up circuit, all other digital circuits are powered off, and the FLASH is powered off. The system wakes up from Standby mode will generate a reset, and SBF (PWR_CSR) will be set at the same time. After waking up, check the SBF status to know the low-power mode before waking up. SBF is cleared by the CSBF (PWR_CR) bit. In the Standby mode, the contents of 32KB of SRAM can be kept (depending on the planning and configuration before going to bed), and the contents of the backup registers are kept.
Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, a rising edge on the WKUP pin, where EXTI signal includes one of 16 external I/O ports, RTC alarm clock,

Ethernet Wake-up signal, USB Wake-up signal.

2.5.7 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In many applications, CRC-based technology is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, a means of detecting flash errors is provided. The CRC calculation unit can be used to calculate the signature of the software in real time and compare it with the signature generated when the software is linked and generated.

2.5.8 Nested vector interrupt controller (NVIC)

The system product has a built-in nested vector interrupt controller (NVIC), which manages 88 maskable interrupt channels and 16 core interrupt channels. And 16 priority levels can be configured.

- Tightly coupled NVIC enables low latency interrupt response processing
- Vectorized interrupt design implements vector entry address directly into the core
- 16 levels of nesting, dynamic modification
- Allow early processing of interrupts
- Support late arrival of higher priority interrupt responses
- Support for break tail link function
- Provide first response to unmaskable interruptions
- Automatic stacking and recovery on interrupt entry and exit, no additional instruction overhead

The module provides flexible interrupt management capabilities with minimal interrupt latency.

2.5.9 External interrupt/event controller (EXTI)

The external interrupt/event controller contains a total of 19 edge detectors for generating interrupt/event requests. Each interrupt line can independently configure its trigger event (rising edge or falling edge or both edges), and can be individually masked; the suspend register maintains all interrupt request states. EXTI can detect that the pulse width is smaller than the clock period of the internal APB2. Up to 53 general-purpose I/O ports can be connected to 16 external interrupt lines.

2.5.10 General-purpose DMA controller

The system has built-in 1 group of general-purpose DMA controllers, manages 8 channels in total, and flexibly handles high-speed data transmission from memory to memory, peripherals to memory, and memory to peripherals, and supports ring buffer mode. Each channel has a dedicated hardware DMA request logic to support one or more peripherals' access requests to the memory. The access priority, transfer length, source address and destination address of the transfer can be configured.

The main peripherals used by DMA include: general-purpose/advanced-control/basic timers TIMx, DAC, USART, I²C and SPI.

Note: DMA and CPU access the system SRAM after arbitration by the arbiter.

2.5.11 Clock and Boot

The system clock source HSI is turned on by default. After the clock is not configured or reset, the internal 8MHz RC oscillator is used as the default CPU clock, and then an external 32MHz clock or PLL clock can be additionally selected. When the clock security mode is turned on, if the HSE is used as the system clock (directly or indirectly), the system clock will automatically switch to the internal RC oscillator when the external clock is detected to be invalid, and the HSE and PLL will be automatically turned off at the same

time; in low-power consumption mode, the system will automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

Multiple prescalers are used to configure the frequency of AHB. The high-speed APB (APB2) and low-speed APB (APB1) regions provide peripheral clocks with a maximum frequency of 144MHz. Refer to the clock tree block diagram in Figure 2-3.

2.5.12 Real time clock (RTC) and backup registers

The RTC and the backup register are in the backup power supply area inside the system. When V_{DD} is valid, it is powered by V_{DD}, and when V_{DD} is invalid, the internal power is automatically switched to the V_{BAT} pin.

The RTC real-time clock is a set of 32-bit programmable counters, and the time base supports 20-bit prescaler for measurement in a longer period of time. The clock reference source is a high-speed external clock divided by 128 (HSE/128), external crystal low-frequency oscillator (LSE) or internal low-power RC oscillator (LSI). The LSE also has a backup power supply area, so when the LSE is selected as the RTC time base, the RTC setting and time can remain unchanged after the system resets or wakes up from Standby mode.

The backup register contains up to 42 16-bit registers, which can be used to store 84 bytes of user application data. This data can continue to be maintained after wake-up from Standby, or system Reset or power Reset. When the intrusion detection function is turned on, once the intrusion detection signal is valid, all contents in the backup register will be cleared.

2.5.13 Analog-to-digital converter (ADC) and touch key capacitance detection (TKey)

The product is embedded with a 12-bit analog/digital converter (ADC), sharing up to 16 external channels and 2 internal channels for sampling. The programmable channel sampling time can realize single, continuous, scanning or discontinuous conversion. And supports dual ADC conversion mode. The analog watchdog function is provided to allow very precise monitoring of one or more selected channels for monitoring the signal voltage of the channel. It supports external event-triggered conversion, the trigger source includes the internal signal and external pin of the on-chip timer; it also supports the use of DMA operations.

ADC internal channel sampling includes 1 channel of built-in temperature sensor sampling and 1 channel of internal reference power sampling. The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the IN16 input channel, which is used to convert the output of the sensor to a digital value.

The capacitance touch key detection unit provides up to 16 detection channels, multiplexing the external channels of the ADC module. The detection result is converted and output by the ADC module, and the state of the touch key is recognized by the user software.

2.5.14 Timer and watchdog

The timers in the system include advanced-control timers, general-purpose timers, basic timers, watchdog timers, and system time base timers. The number of timers included in different products in the series is different, please refer to Table 2-2 for details.

Table 2-2 Timer comparison

Timer		Resolution	Count Type	Time Base	DMA	Function
Advanced-control timer	TIM1	16 bits	Up Down Up/down	APB2 time domain 16-bit divider	Support	PWM complementary output, single pulse output Input capture Output compare Timer count
General-purpose timer	TIM2	16 bits	Up Down Up/down	APB1 time domain 16-bit divider	Support	Input capture Output compare Timer count
	TIM3					
	TIM4					
	TIM5	32 bits				
Window watchdog		7 bits	Down	APB1 time domain 4 types of frequency division	Not support	Timing Reset the system (normal work)
Independent watchdog		12 bits	Down	APB1 time domain 7 types of frequency division	Not support	Timing Reset the system (normal work + low-power work)
SysTick Timer		24 bits	Down	SYSCLK or SYSCLK/8	Not support	Timing

- Advanced-control timer

The advanced-control timer is a 16-bit auto-loading up/down counter with a 16-bit programmable prescaler. In addition to the complete general-purpose timer function, it can be regarded as a three-phase PWM generator distributed to 6 channels, with a complementary PWM output function with dead zone insertion, allowing the timer to be updated after a specified number of counter cycles to repeat counting cycle, braking function, etc. Many functions of the advanced-control timer are the same as the general timer, and the internal structure is also the same. Therefore, the advanced-control timer can cooperate with other TIM timers through the timer link function to provide synchronization or event link functions.

- General-purpose timer

The general-purpose timer is a 16-bit or 32-bit auto-loading up/down counter with a programmable 16-bit prescaler and 4 independent channels. Each channel supports input capture, output comparison, and PWM generation and single pulse mode output. It can also work with advanced-control timers through the timer link function to provide synchronization or event link functions. In Debug mode, the counter can be frozen while the PWM outputs are disabled, thereby cutting off the switches controlled by these outputs. Any general-purpose timer can be used to generate PWM output. Each timer has an independent DMA request mechanism. These timers can also process signals from incremental encoders, as well as digital outputs from 1 to 3 Hall sensors.

- Independent watchdog

The independent watchdog is a configurable 12-bit down counter that supports 7 frequency division factors. The clock is provided by an internal independent 40 KHz RC oscillator (LSI); because the LSI is independent of the main clock, it can run in Stop and Standby modes. IWDG is outside the main program and can work completely independently. Therefore, it is used to reset the entire system when a problem occurs, or as a free timer to provide timeout management for the application. It can be configured as software or hardware to start the watchdog through the option byte. In Debug mode, the counter can be frozen.

- Window Watchdog

The window watchdog is a 7-bit down counter and can be set to free-running. It can be used to reset the entire system when a problem occurs. It is driven by the main clock and has an early warning interrupt function; in Debug mode, the counter can be frozen.

- SysTick Timer

This is a 24-bit optional increment or decrement counter that comes with the core controller. It is used to generate SYSTICK anomalies (exception number: 15). It can be dedicated to the real-time operating system (RTOS) to provide a "heartbeat" tick for the system, or it can be used as a standard 24-bit counter. It has an automatic reload function and a programmable clock source.

2.5.15 Communication interface

2.5.15.1 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The product provides 3 groups of Universal Synchronous/Asynchronous Receiver Transmitters (USART1, USART2, USART3), and 1 groups of Universal Asynchronous Receiver Transmitters (UART4). It supports full-duplex asynchronous communication, synchronous one-way communication and half-duplex single-wire communication. It also supports LIN (Local Interconnect Network), compatible with ISO7816 smart card protocol and IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation. It also allows multi-processor communication. It uses a fractional baud rate generator system and supports DMA operation continuous communication.

2.5.15.2 Serial Peripheral Interface (SPI)

Up to 2 groups of serial peripherals interface (SPI) provide master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8 or 16-bit selection, hardware CRC generation/check for reliable communication, and continuous communication support for DMA operation.

2.5.15.3 I2C bus

Up to 2 I²C bus interfaces can work in multi-master mode or Slave mode, perform all I²C Bus specific timing, protocol, arbitration, etc. It supports both standard and fast speed, and is compatible with SMBus2.0.

The I²C interface provides 7-bit or 10-bit addressing, and supports dual slave addressing in 7-bit Slave mode. It integrates built-in hardware CRC generator/checker. It also supports DMA operation and supports SMBus bus version 2.0 / PMBus bus.

2.5.15.4 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B (active), the baud rate is up to 1Mbits/s, and it supports time-triggered communication functions. It can receive and send standard frames with 11-bit

identifiers, as well as extended frames with 29-bit identifiers. It has 3 sending mailboxes and 2 3-level deep receiving FIFOs.

With 1 set of CAN controller products, there are only 14 configurable filters, and share a dedicated 512-byte SRAM memory with the USBD module for data transmission and reception. When USBD and CAN are used at the same time, in order to prevent access to SRAM conflicts, USBD can only use the lower 384 bytes.

2.5.15.5 Universal Serial Bus device (USBD)

The product is embedded with a USB2.0 full-speed controller, which complies with the USB2.0 full-speed standard. USBD provides 16 configurable USB device endpoints, supports low-speed devices and full-speed devices, supports control/batch/synchronization/interrupt transmission, double buffer mechanism, USB suspend/resume operations, and has standby/wake-up functions. The USB dedicated 48MHz clock is directly generated by the internal main PLL frequency division.

2.5.15.6 Universal Serial Bus USB2.0 full-speed Host/Device controller (USBFS)

The USB2.0 full-speed host controller and device controller (USBFS) follow the USB2.0 full-speed standard. It provides 16 configurable USB device endpoints and a set of host endpoints. Support control/batch/synchronization/interrupt transmission, double buffer mechanism, USB bus suspend/resume operation, and provide standby/wake-up functions. The 48MHz clock dedicated to the USBFS module is directly generated by the internal main PLL frequency division (the PLL must be 144MHz or 96MHz or 48MHz).

2.5.16 General-purpose input and output (GPIO)

The system provides 4 groups of GPIO ports with a total of 53 GPIO pins. Each pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals. Except for ports with analog input functions, all GPIO pins have high current passing capabilities. A locking mechanism is provided to freeze the I/O configuration to avoid accidental writing to the I/O register.

Most of the I/O pins in the system are provided by V_{IO}. Changing the V_{IO} power supply will change the high value of the I/O pin output level to adapt to the external communication interface level. Please refer to the pin description for specific pins.

2.5.17 Operational amplifier/comparator (OPA)

The product has built-in 2 groups of operational amplifiers/comparators, and the internal selection is linked to the ADC and TIMx peripherals. Its input and output can be selected by changing the configuration to select multiple channels. It supports to amplify the external analog small signal and send it to the ADC to realize the small signal ADC conversion. It can also complete the signal comparator function. The comparison result is output by GPIO or directly connected to the input channel of TIMx.

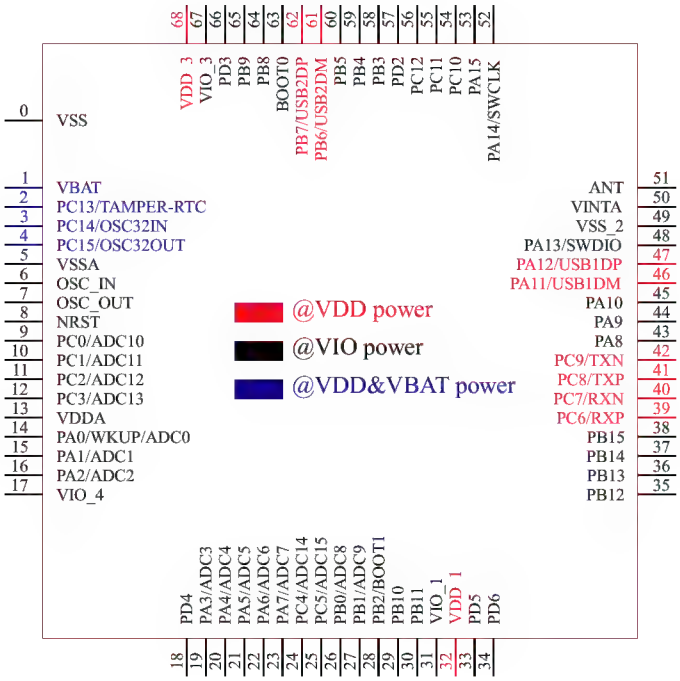
2.5.18 Serial debug interface (SDI)

The core comes with a serial 2-wire debug interface, including SWDIO and SWCLK pins. After the system is powered on or reset, the debug interface pin function is enabled by default.

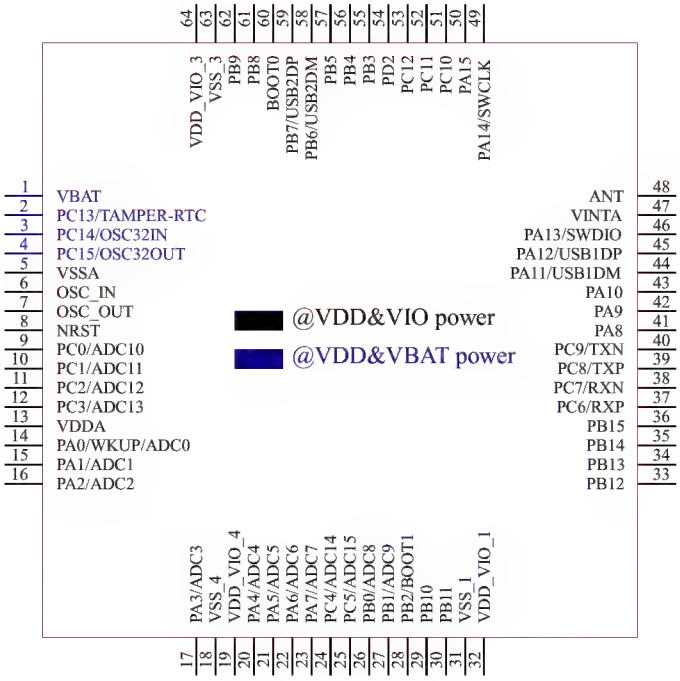
Chapter 3 Pinouts and pin definition

3.1 Wireless device F208 pin arrangement

CH32F208WBU6



CH32F208RBT6



3.2 Pin description

Table 3-1 CH32F208xx pin definitions

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Pin No.		Pin name	Pin type (1)	I/O level	Main function (after reset)	Default alternate function	Remapping function
LQFP64	QFN68						
-	0	V_{SS}	P	-	V_{SS}		
1	1	V_{BAT}	P	-	V_{BAT}		
2	2	PC13-TAMPER-RTC(2)	I/O	-	PC13(3)	TAMPER-RTC	
3	3	PC14-OSC32_IN(2)	I/O/A	-	PC14(3)	OSC32_IN	
4	4	PC15-OSC32_OUT(2)	I/O/A	-	PC15(3)	OSC32_OUT	
5	5	V_{SSA}	P	-	V_{SSA}		
6	6	OSC_IN	I/A	-	OSC_IN		
7	7	OSC_OUT	O/A	-	OSC_OUT		
8	8	NRST	I	-	NRST		
9	9	PC0	I/O/A	-	PC0	ADC_IN10	
10	10	PC1	I/O/A	-	PC1	ADC_IN11	
11	11	PC2	I/O/A	-	PC2	ADC_IN12	
12	12	PC3	I/O/A	-	PC3	ADC_IN13	
13	13	V_{DDA}	P	-	V_{DDA}		
14	14	PA0-WKUP	I/O/A	-	PA0	WKUP/USART2_CTS ADC_IN0/TIM2_CH1 TIM2_ETR/TIM5_CH1	TIM2_CH1_ETR_2
15	15	PA1	I/O/A	-	PA1	USART2_RTS/ADC_IN1 TIM5_CH2/TIM2_CH2	TIM2_CH2_2
16	16	PA2	I/O/A	-	PA2	USART2_TX/TIM5_CH3 ADC_IN2/TIM2_CH3 OPA2_OUT0	TIM2_CH3_1
-	17	V_{IO_4}	P	-	V_{IO_4}		
-	18	PD4	I/O	FT	PD4		
17	19	PA3	I/O/A	-	PA3	USART2_RX/TIM5_CH4 ADC_IN3/TIM2_CH4 OPA1_OUT0	TIM2_CH4_1
18	-	V_{SS_4}	P	-	V_{SS_4}		
19	-	$V_{DD_IO_4}$	P	-	$V_{DD_IO_4}$		
20	20	PA4	I/O/A	-	PA4	SPI1_NSS/USART2_CK	

Pin No.		Pin name	Pin type (1)	I/O level	Main function (after reset)	Default alternate function	Remapping function
LQFP64	QFN68						
						ADC_IN4/OPA2_OUT1	
21	21	PA5	I/O/A	-	PA5	SPI1_SCK/ADC_IN5 OPA2_CH1N	USART1_CTS_2 USART1_CK_3
22	22	PA6	I/O/A	-	PA6	SPI1_MISO/ADC_IN6 TIM3_CH1/OPA1_CH1N	TIM1_BKIN_1 USART1_TX_3
23	23	PA7	I/O/A	-	PA7	SPI1_MOSI/ADC_IN7 TIM3_CH2/OPA2_CH1P	TIM1_CH1N_1 USART1_RX_3
24	24	PC4	I/O/A	-	PC4	ADC_IN14	USART1_CTS_3
25	25	PC5	I/O/A	-	PC5	ADC_IN15	USART1_RTS_3
26	26	PB0	I/O/A	-	PB0	ADC_IN8/TIM3_CH3 OPA1_CH1P	TIM1_CH2N_1 TIM3_CH3_2 UART4_TX_1
27	27	PB1	I/O/A	-	PB1	ADC_IN9 TIM3_CH4 OPA1_OUT1	TIM1_CH3N_1 TIM3_CH4_2 UART4_RX_1
28	28	PB2	I/O	FT	PB2/BOOT1		
29	29	PB10	I/O/A	FT	PB10	I^2C2_SCL/USART3_TX OPA2_CH0N	TIM2_CH3_2 TIM2_CH3_3
30	30	PB11	I/O/A	FT	PB11	I^2C2_SDA/USART3_RX OPA1_CH0N	TIM2_CH4_2 TIM2_CH4_3
31	-	V_{SS_1}	P		V_{SS_1}		
32	-	V_{DD_I/O_1}	P		V_{DD_I/O_1}		
-	31	V_{I/O_1}	P		V_{I/O_1}		
-	32	V_{DD_1}	P		V_{DD_1}		
-	33	PD5	I/O	FT	PD5		
	34	PD6	I/O	FT	PD6		
33	35	PB12	I/O/A	FT	PB12	SPI2_NSS/I^2C2_SMBA USART3_CK/TIM1_BKIN	
34	36	PB13	I/O/A	FT	PB13	SPI2_SCK/USART3_CTS TIM1_CH1N	USART3_CTS_1
35	37	PB14	I/O/A	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS/OPA2_CH0P	USART3_RTS_1
36	38	PB15	I/O/A	FT	PB15	SPI2_MOSI/TIM1_CH3N OPA1_CH0P	USART1_TX_2
37	39	PC6	I/O	FT	PC6	ETH_RXP	TIM3_CH1_3
38	40	PC7	I/O	FT	PC7	ETH_RXN	TIM3_CH2_3
39	41	PC8	I/O	FT	PC8	ETH_TXP	TIM3_CH3_3
40	42	PC9	I/O	FT	PC9	ETH_TXN	TIM3_CH4_3
41	43	PA8	I/O	FT	PA8	USART1_CK TIM1_CH1/MCO	USART1_CK_1 USART1_RX_2

Pin No. LQFP64	Pin No. QFN68	Pin name	Pin type (1)	I/O level	Main function (after reset)	Default alternate function	Remapping function
							TIM1_CH1_1
42	44	PA9	I/O	FT	PA9	USART1_TX TIM1_CH2	USART1_RTS_2 TIM1_CH2_1
43	45	PA10	I/O	FT	PA10	USART1_RX TIM1_CH3	USART1_CK_2 TIM1_CH3_1
44	46	PA11	I/O/A	FT	PA11	USART1_CTS/USBDM CAN1_RX/TIM1_CH4	USART1_CTS_1 TIM1_CH4_1
45	47	PA12	I/O/A	FT	PA12	USART1_RTS/USBDP CAN1_TX/TIM1_ETR	USART1_RTS_1 TIM1_ETR_1
46	48	PA13	I/O	FT	SWDIO		PA13
-	49	V_{SS_2}	P	-	V_{SS_2}		
47	50	V_{INTA}	P	-	V_{INTA}		
48	51	ANT	A	-	ANT		
49	52	PA14	I/O	FT	SWCLK		PA14
50	53	PA15	I/O	FT	PA15		TIM2_CH1_ETR_1 TIM2_CH1_ETR_3 SPI1_NSS
51	54	PC10	I/O	FT	PC10	UART4_TX	USART3_TX_1
52	55	PC11	I/O	FT	PC11	UART4_RX	USART3_RX_1
53	56	PC12	I/O	FT	PC12		USART3_CK_1
54	57	PD2	I/O	FT	PD2	TIM3_ETR	TIM3_ETR_2 TIM3_ETR_3
55	58	PB3	I/O	FT	PB3		TRACESWO TIM2_CH2_1 TIM2_CH2_3 SPI1_SCK
56	59	PB4	I/O	FT	PB4		TIM3_CH1_2 SPI1_MISO
57	60	PB5	I/O	-	PB5	I^2C1_SMBA	TIM3_CH2_2 SPI1_MOSI
58	61	PB6	I/O	FT	PB6	I^2C1_SCL/TIM4_CH1 USBFS_DM	USART1_TX_1
59	62	PB7	I/O	FT	PB7	I2C1_SDA TIM4_CH2/USBFS_DP	USART1_RX_1
60	63	BOOT0	I	-	BOOT0		
61	64	PB8	I/O/A	FT	PB8	TIM4_CH3	I^2C1_SCL/CAN1_RX
62	65	PB9	I/O/A	FT	PB9	TIM4_CH4	I^2C1_SDA/CAN1_TX
-	66	PD3	I/O	FT	PD3		
63	-	V_{SS_3}	P	-	V_{SS_3}		
64	-	V_{DD_I/O_3}	P	-	V_{DD_I/O_3}		

Pin No.		Pin name	Pin type (1)	I/O level	Main function (after reset)	Default alternate function	Remapping function
LQFP64	QFN68						
-	67	V_{I/O_3}	P	-	V_{I/O_3}		
-	68	V_{DD_3}	P	-	V_{DD_3}		

Note 1: Abbreviations in the table

I = TTL/CMOS Schmitt input;

O = CMOS tri-state output;

A = analog signal input or output;

P = power;

FT = 5V tolerance;

ANT = RF signal input and output (antenna);

Note 2: The PC13, PC14 and PC15 pins are powered by the power switch, and this power switch can only absorb a limited current (3mA). Therefore, when these 3 pins are used as output pins, there are the following restrictions: only one pin can be used as an output at the same time. When used as an output pin, it can only work in 2MHz mode. The maximum drive load is 30pF and cannot be used as a current source (Such as driving LED).

Note 3: These pins are in the main function state when the backup area is powered on for the first time. Even after reset, the state of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these I/O ports, please refer to the relevant chapters on the battery backup area and BKP register in the CH32xRM.

Note 4: Pin 5 and pin 6 of those in LQFP64M package are configured as OSC_IN and OSC_OUT function pins by default after chip reset. Software can reconfigure these 2 pins as PD0 and PD1.

Note 5: For devices without the BOOT0 pinout, they are pulled down to GND internally. For devices with the BOOT0 pinout but no BOOT1/PB2 pinout, BOOT1/PB2 is pulled down to GND internally. At this time, if you enter the low-power mode to configure the I/O port state, it is recommended that the BOOT1/PB2 pins use the input pull-down mode to prevent additional current generation.

3.3 Pin alternate functions

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Table 3-2 CH32F208xx alternate function pin definitions

Alternate / Pin	ADC	TIM1	TIM2/3/4/5	UART/USART	USB	SYS	I²C	SPI	ETH	OPA	CAN
PA0	ADC_IN0		TIM2_CH1 TIM2_ETR TIM2_CH1_ETR_2 TIM5_CH1	USART2_CTS		WKUP					
PA1	ADC_IN1		TIM2_CH2 TIM2_CH2_2 TIM5_CH2	USART2_RTS							
PA2	ADC_IN2		TIM2_CH3 TIM2_CH3_1 TIM5_CH3	USART2_TX						OPA2_OUT0	
PA3	ADC_IN3		TIM2_CH4 TIM2_CH4_1 TIM5_CH4	USART2_RX						OPA1_OUT0	
PA4	ADC_IN4			USART2_CK				SPI1_NSS		OPA2_OUT1	
PA5	ADC_IN5			USART1_CTS_2 USART1_CK_3				SPI1_SCK		OPA2_CH1N	
PA6	ADC_IN6	TIM1_BKIN_1	TIM3_CH1	USART1_TX_3				SPI1_MISO		OPA1_CH1N	
PA7	ADC_IN7	TIM1_CH1N_1	TIM3_CH2	USART1_RX_3				SPI1_MOSI		OPA2_CH1P	
PA8		TIM1_CH1 TIM1_CH1_1		USART1_CK USART1_CK_1 USART1_RX_2		MCO					
PA9		TIM1_CH2 TIM1_CH2_1		USART1_TX USART1_RTS_2							
PA10		TIM1_CH3 TIM1_CH3_1		USART1_RX USART1_CK_2							
PA11		TIM1_CH4 TIM1_CH4_1		USART1_CTS USART1_CTS_1	USBDM						CAN1_RX
PA12		TIM1_ETR TIM1_ETR_1		USART1_RTS USART1_RTS_1	USBDP						CAN1_TX
PA13						SWDIO					
PA14						SWCLK					
PA15			TIM2_CH1_ETR_1 TIM2_CH1_ETR_3					SPI1_NSS			
PB0	ADC_IN8	TIM1_CH2N_1	TIM3_CH3 TIM3_CH3_2	UART4_TX_1						OPA1_CH1P	
PB1	ADC_IN9	TIM1_CH3N_1	TIM3_CH4 TIM3_CH4_2	UART4_RX_1						OPA1_OUT1	
PB2						BOOT1					
PB3			TIM2_CH2_1 TIM2_CH2_3					SPI1_SCK			
PB4			TIM3_CH1_2					SPI1_MISO			
PB5			TIM3_CH2_2				I²C1_SMBA	SPI1_MOSI			
PB6			TIM4_CH1	USART1_TX_1	USBFS_DM		I²C1_SCL				
PB7			TIM4_CH2	USART1_RX_1	USBFS_DP		I²C1_SDA				

Alternate / Pin	ADC	TIM1	TIM2/3/4/5	UART/USART	USB	SYS	I²C	SPI	ETH	OPA	CAN
PB8			TIM4_CH3				I²C1_SCL				CAN1_RX
PB9			TIM4_CH4				I²C1_SDA				CAN1_TX
PB10			TIM2_CH3_2 TIM2_CH3_3	USART3_TX			I²C2_SCL			OPA2_CH0N	
PB11			TIM2_CH4_2 TIM2_CH4_3	USART3_RX			I²C2_SDA			OPA1_CH0N	
PB12		TIM1_BKIN		USART3_CK			I²C2_SMBA	SPI2_NSS			
PB13		TIM1_CH1N		USART3_CTS USART3_CTS_1				SPI2_SCK			
PB14		TIM1_CH2N		USART3_RTS USART3_RTS_1				SPI2_MISO		OPA2_CH0P	
PB15		TIM1_CH3N		USART1_TX_2				SPI2_MOSI		OPA1_CH0P	
PC0	ADC_IN10										
PC1	ADC_IN11										
PC2	ADC_IN12										
PC3	ADC_IN13										
PC4	ADC_IN14			USART1_CTS_3							
PC5	ADC_IN15			USART1_RTS_3							
PC6			TIM3_CH1_3						ETH_RXP		
PC7			TIM3_CH2_3						ETH_RXN		
PC8			TIM3_CH3_3						ETH_TXP		
PC9			TIM3_CH4_3						ETH_TXN		
PC10				UART4_TX USART3_TX_1							
PC11				UART4_RX USART3_RX_1							
PC12				USART3_CK_1							
PC13						TAMPER_RTC					
PC14						OSC32_IN					
PC15						OSC33_OUT					
PD2			TIM3_ETR TIM3_ETR_2 TIM3_ETR_3								

Chapter 4 Electrical characteristics

4.1 Test conditions

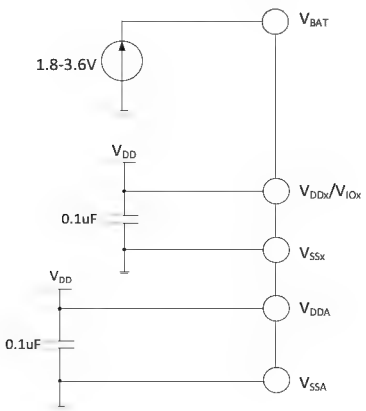
Unless otherwise specified and marked, all voltages are referenced to V_{SS}.

All minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency. Typical values are based on normal temperature (25°C) and V_{DD} = 3.3V environment, which are given only as design guidelines.

The data based on comprehensive evaluation, design simulation or technology characteristics are not tested in production. On the basis of comprehensive evaluation, the minimum and maximum values refer to sample tests. Unless otherwise specified that is tested, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 4-1 Typical circuit for conventional power supply



4.2 Absolute maximum ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Table 4-1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
T_A	Ambient temperature during operation	-40	85	°C
T_S	Ambient temperature during storage	-40	125	°C
V_{DD}-V_{SS}	External main supply voltage (includingV_{DDA} and V_{DD})	-0.3	4.0	V
V_{IO}-V_{SS}	I/O domain supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on the FT (5V tolerance) pin	V_{SS}-0.3	5.5	V
	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	
$\lvert\triangle V_{DD_x}\rvert$	Variations between different main power supply pins		50	mV
$\lvert\triangle V_{IO_x}\rvert$	Variations between different I/O power supply pins		50	mV

$\lvert\triangle V_{SS_x}\rvert$	Variations between different ground pins		50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model, non-contact)	4K		V
	USB pins (PA11, PA12)	3K		V
I_{VDD}	Total current into $V_{DD}/V_{DDA}/V_{I/O}$ power lines (supply current)		150	mA
I_{Vss}	Total current out of V_{SS} ground lines (outflow current)		150	
$I_{I/O}$	Sink current on any I/O and control pin		25	
	Output current on any I/O and control pin		-25	
$I_{INJ(PIN)}$	Injected current on NRST pin		+/-5	
	Injected current on HSE's OSC_IN pin and LSE's OSC_IN pin		+/-5	
	Injected current on other pins		+/-5	
$\sum I_{INJ(PIN)}$	Total injected current on all I/Os and control pins		+/-25	

4.3 Electrical characteristics

4.3.1 Operating conditions

Table 4-2 General operating conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
F_{HCLK}	Internal AHB clock frequency			144	MHz
F_{PCLK1}	Internal APB1 clock frequency			144	MHz
F_{PCLK2}	Internal APB2 clock frequency			144	MHz
V_{DD}	Standard operating voltage		2.4	3.6	V
		Use USB or ETH	3.0	3.6	
$V_{I/O}$	Output voltage on most I/O pins	$V_{I/O}$ cannot be more than V_{DD}	2.4	3.6	V
V_{DDA}	Analog operating voltage (ADC is not used)	V_{DDA} must be the same as $V_{I/O}$, V_{REF+} cannot be higher than V_{DDA}, V_{REF-} is equal to V_{SS}.	2.4	3.6	V
	Analog operating voltage (ADC is used)				
V_{BAT}(1)	Backup operating voltage	Cannot be more than V_{DD}	1.8	3.6	V
T_A	Ambient temperature		-40	85	℃
T_J	Junction temperature range		-40	85	℃

Note: 1. The connection line from the battery to V_{BAT} should be as short as possible.

Table 4-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	us/V
	V_{DD} fall time rate		30	∞	

4.3.2 Embedded reset and power control block characteristics

Table 4-4 Reset and voltage monitor (For PDR, select high threshold gear)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PVD}(1)	Programmable voltage detector level selection	PLS[2:0] = 000 (rising edge)		2.39		V
		PLS[2:0] = 000 (falling edge)		2.31		V
		PLS[2:0] = 001 (rising edge)		2.56		V
		PLS[2:0] = 001 (falling edge)		2.48		V
		PLS[2:0] = 010 (rising edge)		2.65		V
		PLS[2:0] = 010 (falling edge)		2.57		V
		PLS[2:0] = 011 (rising edge)		2.78		V
		PLS[2:0] = 011 (falling edge)		2.69		V
		PLS[2:0] = 100 (rising edge)		2.89		V
		PLS[2:0] = 100 (falling edge)		2.81		V
		PLS[2:0] = 101 (rising edge)		3.05		V
		PLS[2:0] = 101 (falling edge)		2.96		V
		PLS[2:0] = 110 (rising edge)		3.17		V
		PLS[2:0] = 110 (falling edge)		3.08		V
		PLS[2:0] = 111 (rising edge)		3.31		V
		PLS[2:0] = 111 (falling edge)		3.21		V
$V_{PVDhyst}$	PVD hysteresis			0.08		V
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge	1.9	2.2	2.4	V
		Falling edge	1.9	2.2	2.4	V
$V_{PDRhyst}$	PDR hysteresis			20		mV
$t_{RSTTEMPO}$	Power on reset		24	28	30	mS
	Other resets		8	10	30	

Note: 1. Normal temperature test value.

4.3.3 Embedded reference voltage

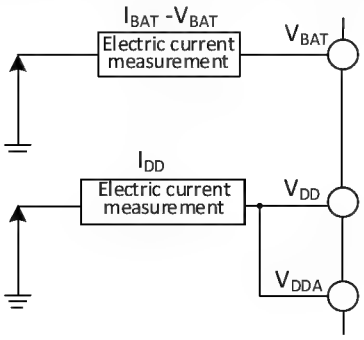
Table 4-5 Embedded reference voltage

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	T_A = -40°C~85°C	1.17	1.2	1.23	V
$T_{S_vrefint}$	ADC sampling time when reading the internal reference voltage				17.1	us

4.3.4 Supply current characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, the software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 4-2 Current consumption measurement



The microcontroller is in the following conditions:

Under normal temperature conditions and when V_{DD} = 3.3V, all I/O ports are configured with pull-up inputs, only one of HSE and HIS is enabled, HSE=32M, HIS=8M (calibrated), F_{PLCK1}=F_{HCLK}, F_{PLCK2}=F_{HCLK}, PLL is enabled when FHCLK>8MHz. Enable or disable the power consumption of all peripheral clocks.

Table 4-6-1 Typical current consumption in Run mode, the data processing code runs from the internal Flash

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled(2)	
I_{DD}(1)	Supply current in Run mode	External clock	F_{HCLK} = 144MHz	20.37	14.8	mA
			F_{HCLK} = 72MHz	10.47	7.69	
			F_{HCLK} = 48MHz	7.17	5.32	
			F_{HCLK} = 36MHz	6.1	4.53	
			F_{HCLK} = 24MHz	3.89	2.96	
			F_{HCLK} = 16MHz	3.01	2.32	
			F_{HCLK} = 8MHz	1.7	1.39	
			F_{HCLK} = 4MHz	1.17	1.01	
			F_{HCLK} = 500KHz	0.71	0.68	
		Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency.	F_{HCLK} = 144MHz	19.9	13.63	
			F_{HCLK} = 72MHz	10.22	7.44	
			F_{HCLK} = 48MHz	6.99	5.15	
			F_{HCLK} = 36MHz	5.43	4.14	
			F_{HCLK} = 24MHz	3.79	2.86	
			F_{HCLK} = 16MHz	2.76	2.15	
			F_{HCLK} = 8MHz	1.55	1.21	
			F_{HCLK} = 4MHz	1.02	0.83	
			F_{HCLK} = 500KHz	0.54	0.52	

Note: 1. The above are the actual measured parameters of similar chips, the actual value will be slightly deviated.

Table 4-6-2 BLE power consumption

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$I_{DD(BLE)}$(1)	RX	Under normal temperature		15.2		mA

	TX	-18dBm	V_{DD} = 3.3V		6.28		
		0dBm			12.8		
		+7dBm			35.1		

Note: 1. The above are measured parameters.

Table 4-7 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled(2)	
I_{DD}(1)	Supply current in Sleep mode (In this case, peripheral power supply and clock are maintained)	External clock	F_{HCLK} = 144MHz	9.18	3.52	mA
			F_{HCLK} = 72MHz	4.86	2.03	
			F_{HCLK} = 48MHz	3.44	1.55	
			F_{HCLK} = 36MHz	3.26	1.68	
			F_{HCLK} = 24MHz	2.02	1.07	
			F_{HCLK} = 16MHz	1.75	1.05	
			F_{HCLK} = 8MHz	1.08	0.77	
			F_{HCLK} = 4MHz	0.86	0.69	
			F_{HCLK} = 500KHz	0.66	0.64	
		Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency.	F_{HCLK} = 144MHz	9.23	3.52	
			F_{HCLK} = 72MHz	4.87	2.01	
			F_{HCLK} = 48MHz	3.43	1.53	
			F_{HCLK} = 36MHz	2.88	1.39	
			F_{HCLK} = 24MHz	2.0	1.05	
			F_{HCLK} = 16MHz	1.59	0.93	
			F_{HCLK} = 8MHz	0.92	0.61	
			F_{HCLK} = 4MHz	0.69	0.55	
			F_{HCLK} = 500KHz	0.50	0.48	

Note: 1. The above are the actual measured parameters of similar chips, the actual value will be slightly deviated.

Table 4-8 Typical current consumption in Stop and Standby mode

Symbol	Parameter	Condition	Typ.	Unit
I_{DD}	Supply current in Stop mode	Voltage regulator in Run mode, low-speed and high-speed internal RC oscillators and external oscillators off (no independent watchdog)	253.4	uA
		Voltage regulator in low-power mode, low-speed and high-speed internal RC oscillators and external oscillators off (no independent watchdog, PVD off), RAM enters low-power mode	26.5	

	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog on, all RAM not powered	1.3	
		Low-speed internal RC oscillator on, independent watchdog off, all RAM not powered	1.3	
		LSI/LSE/RTC/IWDG off, 32K_RAM powered and in low-power mode	2.5	
		LSI/LSE/RTC/IWDG off, 2K_RAM powered and in low-power mode	0.9	
		LSI/LSE/RTC/IWDG off, all RAM not powered	0.7	
I_{DD_VBAT}	Backup domain supply current (Remove V_{DD} and V_{DDA}, only powered by V_{BAT}	Low-speed external oscillator and RTC on	1.23	

Note: The above are measured parameters.

4.3.5 External clock source characteristics

Table 4-9 From external high-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSE_ext}	External clock frequency			32		MHz
V_{HSEH}(1)	OSC_IN input pin high level voltage		$0.8V_{I/O}$		$V_{I/O}$	V
V_{HSEL}(1)	OSC_IN input pin low-level voltage		0		$0.2V_{I/O}$	V
$C_{in(HSE)}$	OSC_IN input capacitance			5		pF
$DuCy_{(HSE)}$	Duty cycle			50		%
I_L	OSC_IN input leakage current				±1	uA

Note: 1. Failure to meet this condition may cause level recognition error.

Figure 4-3 External high-frequency clock source circuit

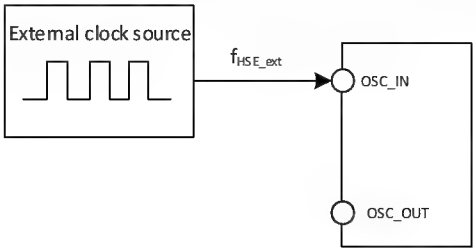


Table 4-10 From external low-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSE_ext}	User external clock frequency			32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level		$0.8V_{DD}$		V_{DD}	V

	voltage					
V_{LSEL}	OSC32_IN input pin low voltage		0		$0.2V_{DD}$	V
$C_{in(LSE)}$	OSC32_IN input capacitance			5		pF
$DuCy_{(LSE)}$	Duty cycle			50		%
I_L	OSC32_IN input leakage current				±1	uA

Figure 4-4 External low-frequency clock source circuit

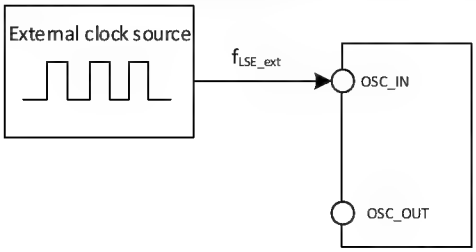


Table 4-11 High-speed external clock generated from a crystal/ceramic resonator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{OSC_IN}	Resonator frequency			32(2)		MHz
R_F	Feedback resistance			250		kΩ
C	Recommended load capacitance and corresponding crystal series impedance R_S	R_S=60Ω(1)		30		pF
I_2	HSE drive current	V_{DD} = 3.3V，20p load		0.53		mA
g_m	Oscillator transconductance	Startup		17.5		mA/V
$t_{SU(HSE)}$	Startup time	V_{DD} is stable, 8M crystal		2.5		ms

Note 1: It is recommended that the ESR of 25M crystal should not exceed 60 Ω, and it can be relaxed if it is lower than 25M.

2. No external load capacitor is required.

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, C_{L1}=C_{L2}, generally C_{L1}=C_{L2}.

For the CH32F208xx series, they are connected with external 32M crystals, and they have built-in load capacitor, so the external circuit is not necessary.

Figure 4-5 Typical circuit of external 32M crystal

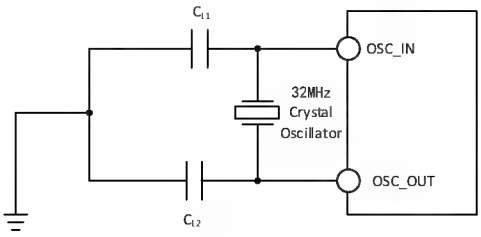


Table 4-12 Low-speed external clock generated by generated from a crystal/ceramic resonator

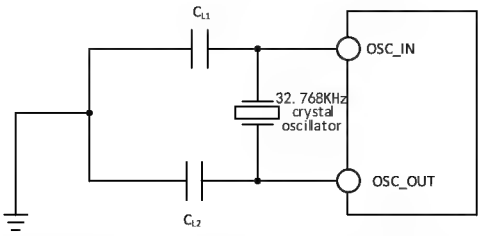
(f(LSE)=32.768KHz)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_F	Feedback resistance			5		MΩ
C	Recommended load capacitance and corresponding crystal serial impedance R_S	R_S<70kΩ			15	pF
i_2	LSE drive current	VDD = 3.3V		0.35		uA
g_m	Oscillator transconductance	Startup		25.3		uA/V
$t_{SU(LSE)}$	Startup time	VDD is stable		800		mS

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, C_{L1}=C_{L2}, generally C_{L1}=C_{L2}, which is optional around 12pF.

Figure 4-6 Typical circuit of external 32.768K crystal



Note: The load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$. C_{stray} is the capacitance of the pin and the PCB board or PCB-related capacitance. Its typical value is between 2pF and 7pF.

4.3.6 Internal clock source characteristics

Table 4-13 Internal high-speed (HSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency (after calibration)			8		MHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator (after calibration)	TA = 0℃～70℃	-1.0		1.6	%
		TA = -40℃～85℃	-2.2		2.2	%
$t_{SU(HSI)}$	HSI oscillator startup stabilization time			10		us
$I_{DD(HSI)}$	HSI oscillator power consumption		120	180	270	uA

Table 4-14 Internal low-speed (LSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		25	32	45	KHz
$DuCy_{LSI}$	Duty cycle		45	50	55	%
ACC_{LSI}	Accuracy of LSI oscillator (after calibration)	Constant temperature within ± 1 ℃, build 10s calibration once		±500		ppm

$t_{SU(LSI)}$	LSI oscillator startup stabilization time			100		us
$I_{DD(LSI)}$	LSI oscillator power consumption			0.6		uA

4.3.7 PLL characteristics

Table 4-15 PLL characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{PLL_IN}	PLL input clock		4	8	25	MHz
	PLL input clock duty cycle		40		60	%
F_{PLL_OUT}	PLL multiplier output clock		40		240(1)	MHz
t_{LOCK}	PLL lock time				200	us

Note 1: The frequency multiplier must be selected to meet the PLL output frequency range.

4.3.8 Wakeup time from low-power mode

Table 4-16 Wakeup time from low-power mode(1)

Symbol	Parameter	Condition	Typ.	Unit
$t_{wusleep}$	Wakeup from Sleep mode	Wake up using HSI RC clock	2.6	us
t_{wustop}	Wakeup from Stop mode (voltage regulator is in Run mode)	Wake on HSI RC clock	23.1	us
	Wakeup from Stop mode (voltage regulator is in low-power mode)	Voltage regulator wakeup time from low-power mode + HSI RC clock wake up	299	us
$t_{WUSTDBY}$	Wakeup from Standby mode	LDO stabilization time + HSI RC clock wake up + code load time(2) (take 128K as example)	5.0	ms

Note: 1. The above parameters are measured parameters, the actual value will be slightly deviated..

2. The code load time is calculated based on the current zero-wait area capacity configured by the chip and the size of the loading configuration clock.

4.3.9 Memory characteristics

Table 4-17 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{prog}	Programming frequency(1)	T_A = -40°C～85°C			60	MHz
t_{prog_page}	Page (256 bytes) programming time	T_A = -40°C～85°C		2		ms
t_{erase_page}	Page (256 bytes) erase time	T_A = -40°C～85°C		16		ms
t_{erase_sec}	Sector (4K bytes) erase time	T_A = -40°C～85°C		16		ms
V_{prog}	Programming voltage		2.4		3.6	V

Note: 1. For the programming frequency of flash, read operation, program operation and erase operation are included. The clock is from HCLK.

Table 4-18 Flash memory endurance and data retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Endurance	T_A = 25℃	10K	80K(1)		times
t_{RET}	Data retention		20			year

Note: The endurance parameter is actual measured, which is not guaranteed.

4.3.10 I/O port characteristics

Table 4-19 General-purpose I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Standard I/O pin, input high level voltage		0.41*(V_{DD}-1.8)+1.3		V_{DD}+0.3	V
	FT I/O pin, input high level voltage		0.42*(V_{DD}-1.8)+1		5.5	V
V_{IL}	Standard I/O pin, input low-level voltage		-0.3		0.28*(V_{DD}-1.8)+0.6	V
	FT I/O pin, input low-level voltage		-0.3		0.32*(V_{DD}-1.8)+0.55	V
V_{hys}	Standard I/O pin Schmitt trigger voltage hysteresis		150			mV
	FT I/O pin Schmitt trigger voltage hysteresis		90			
I_{lkg}	Input leakage current	Standard I/O port			1	uA
		FT I/O port			3	
R_{PU}	Weak pull-up equivalent resistance		30	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistance		30	40	55	kΩ
$C_{I/O}$	I/O pin capacitance			5		pF

Output drive current characteristics

GPIO (General-Purpose Input/Output Port) can sink or output up to ±8mA current, and sink or output ±20mA current (not strictly to V_{OL}/V_{OH}). In user applications, the total driving current of all I/O pins cannot exceed the absolute maximum ratings given in Section 4.2:

Table 4-20 Output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level when 8 pins are sunk	TTL port, $I_{I/O}$ = +8mA		0.4	V
V_{OH}	Output high level when 8 pins are sourced	2.7V< V_{DD} <3.6V	V_{DD}-0.4		
V_{OL}	Output low level when 8 pins are sunk	CMOS port, $I_{I/O}$ = +8mA		0.4	V
V_{OH}	Output high level when 8 pins are sourced	2.7V< V_{DD} <3.6V	2.3		
V_{OL}	Output low level when 8 pins are sunk	$I_{I/O}$ = +20mA		1.3	V
V_{OH}	Output high level when 8 pins are sourced	2.7V< V_{DD} <3.6V	V_{DD}-1.3		
V_{OL}	Output low level when 8 pins are sunk	$I_{I/O}$ = +6mA		0.4	V
V_{OH}	Output high level when 8 pins are sourced	2.4V< V_{DD} <2.7V	V_{DD}-1.3		

Note: In the above conditions, if multiple I/O pins are driven at the same time, the total current cannot exceed

the absolute maximum ratings given in Table 4.2. In addition, when multiple I/O pins are driven at the same time, the current on the power/ground point is very large, which will cause the voltage drop to make the internal I/O voltage not reach the power supply voltage in the table, resulting in the drive current being less than the nominal value.

Table 4-21 Input/output AC characteristics

MODEx[1:0] configuration	Symbol	Parameter	Condition	Min.	Max.	Unit
10 (2MHz)	$F_{max(I/O)out}$	Maximum frequency	CL=50pF,V_{DD}=2.7-3.6V		2	MHz
	$t_{f(I/O)out}$	Output high to low fall time	CL=50pF,V_{DD}=2.7-3.6V		125	ns
	$t_{r(I/O)out}$	Output low to high rise time			125	ns
01 (10MHz)	$F_{max(I/O)out}$	Maximum frequency	CL=50pF,V_{DD}=2.7-3.6V		10	MHz
	$t_{f(I/O)out}$	Output high to low fall time	CL=50pF,V_{DD}=2.7-3.6V		25	ns
	$t_{r(I/O)out}$	Output low to high rise time			25	ns
11 (50MHz)	$F_{max(I/O)out}$	Maximum frequency	CL=30pF,V_{DD}=2.7-3.6V		50	MHz
			CL=50pF,V_{DD}=2.7-3.6V		30	MHz
	$t_{f(I/O)out}$	Output high to low fall time	CL=30pF,V_{DD}=2.7-3.6V		20	ns
			CL=50pF,V_{DD}=2.7-3.6V		5	ns
	$t_{r(I/O)out}$	Output low to high rise time	CL=30pF,V_{DD}=2.7-3.6V		8	ns
			CL=50pF,V_{DD}=2.7-3.6V		12	ns
	t_{EXTIpw}	The EXTI controller detects the pulse width of the external signal		10		ns

4.3.11 NRST pin characteristics

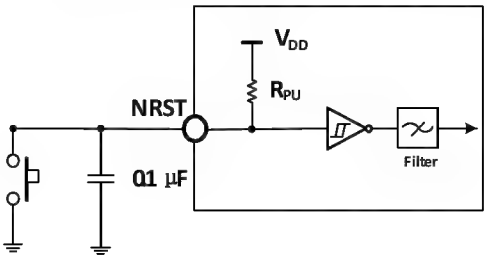
Table 4-22 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low-level voltage		-0.3		0.28*(V_{DD}-1.8)+0.6	V
$V_{IH(NRST)}$	NRST input high-level voltage		0.41*(V_{DD}-1.8)+1.3		V_{DD}+0.3	V
$V_{hys(NRST)}$	NRST Schmitt Trigger voltage hysteresis		150			mV
R_{PU}(1)	Weak pull-up equivalent resistance		30	40	50	kΩ
$V_{F(NRST)}$	NRST input filtered pulse width				100	ns
$V_{NF(NRST)}$	NRST input not filtered pulse width		300			ns

Note: 1. The pull-up resistor is a real resistor in series with a switchable PMOS implementation. The resistance of this PMOS/NMOS switch is very small (approximately 10%).

Circuit reference design and requirements:

Figure 4-7 Typical circuit of external reset pin



4.3.12 TIM timer characteristics

Table 4-23 TIMx characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	13.9		ns
F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72MHz	0	36	MHz
R_{esTIM}	Timer resolution			16	位
$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	0.0139	910	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz		59.6	s

4.3.13 I2C interface characteristics

Figure 4-8 I²C bus timing diagram

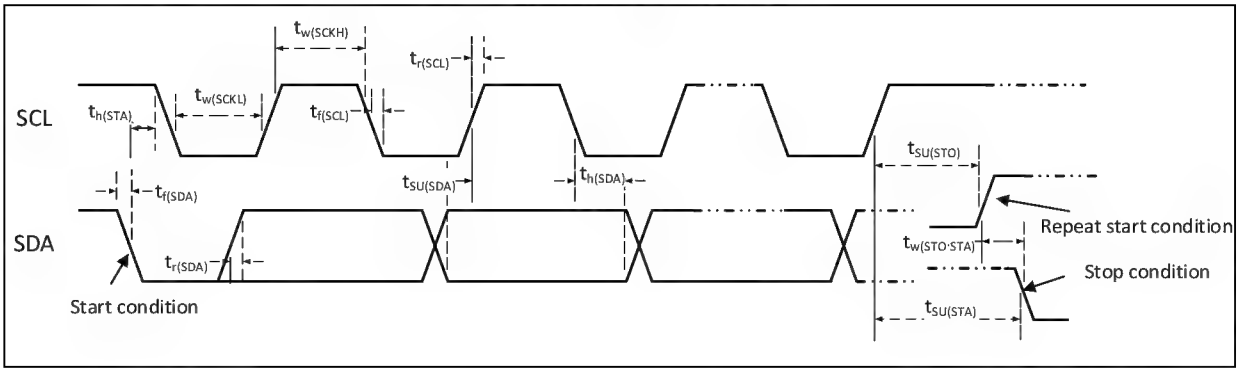


Table 4-24 I²C interface characteristics

Symbol	Parameter	Standard I²C		Fast I²C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time		300			ns

$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us
C_b	Capacitive load for each bus		400		400	pF

4.3.14 SPI interface characteristics

Figure 4-9 SPI timing diagram in Master mode

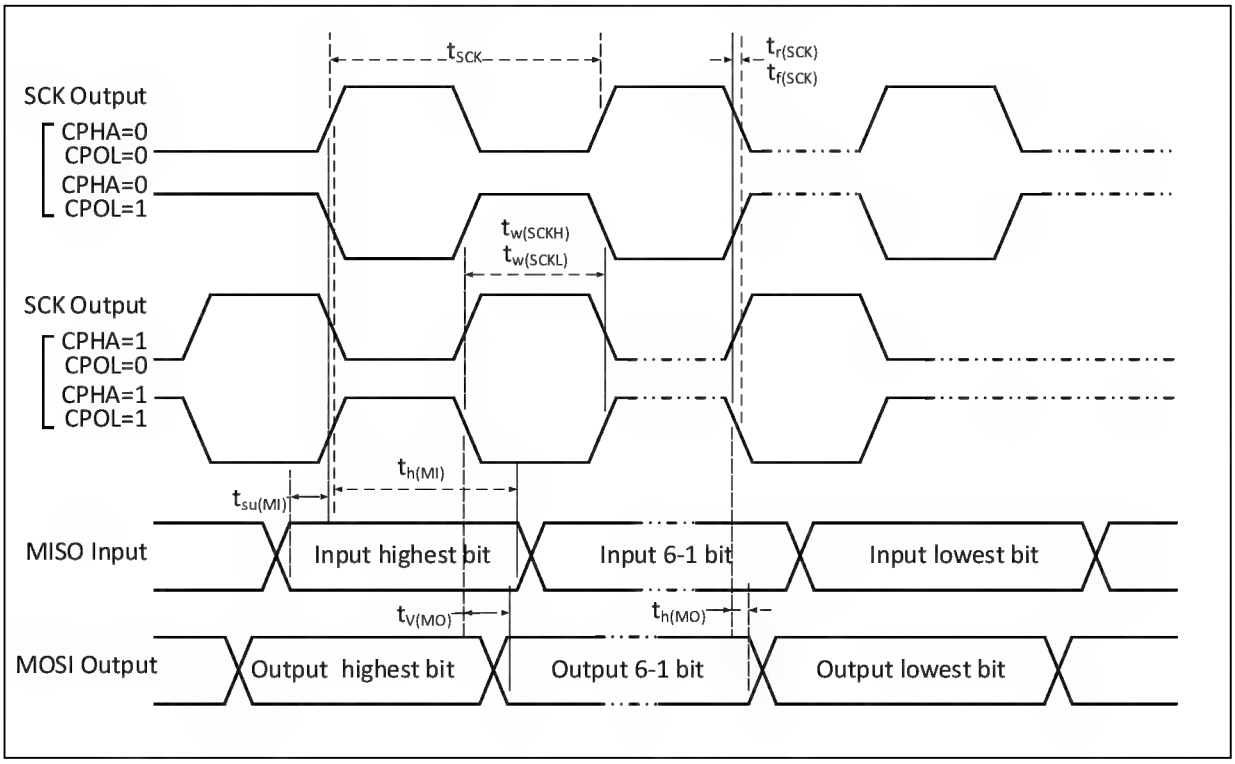


Figure 4-10 SPI timing diagram in Slave mode (CPHA=0)

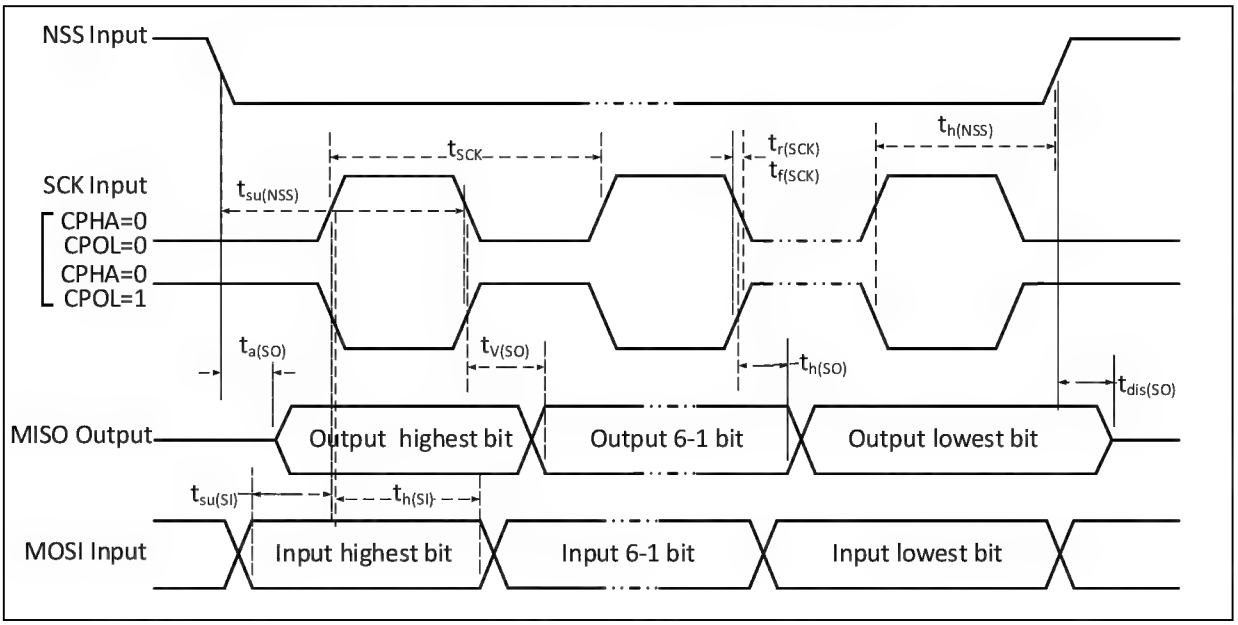


Figure 4-11 SPI timing diagram in Slave mode (CPHA=1)

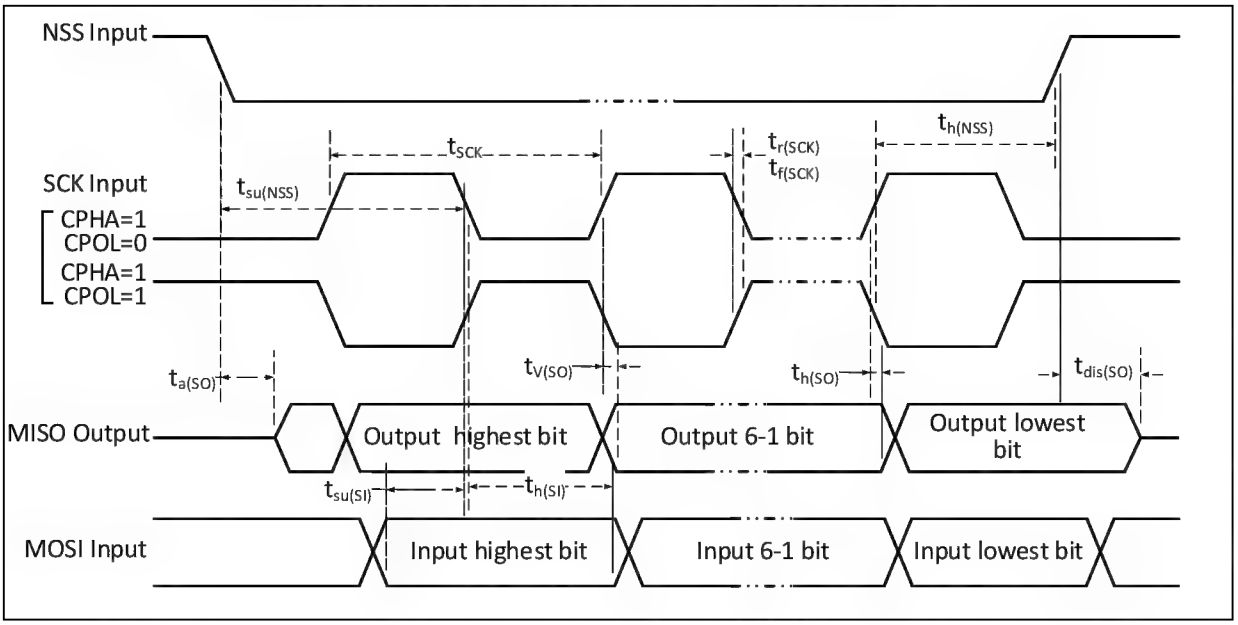


Table 4-25 SPI interface characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCK}/t_{SCK}	SPI clock frequency	Master mode		36	MHz
		Slave mode		36	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance:C = 30pF		20	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode	$2t_{PCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{PCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36MHz,	40	60	ns

		Prescaler factor = 4			
$t_{SU(MI)}$	Data input setup time	Master mode	5		ns
$t_{SU(SI)}$		Slave mode	5		ns
$t_{h(MI)}$	Data input hold time	Master mode	5		ns
$t_{h(SI)}$		Slave mode	4		ns
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20MHz	0	$1t_{PCLK}$	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	0	10	ns
$t_{V(SO)}$	Data output valid time	Slave mode (After enable edge)		25	ns
$t_{V(MO)}$		Master mode (After enable edge)		5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (After enable edge)	15		ns
$t_{h(MO)}$		Master mode (After enable edge)	0		ns

4.3.15 USB interface characteristics

Table 4-26 USB characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{DD}	USB operating voltage		3.0	3.6	V
V_{SE}	Single-ended receiver threshold	V_{DD} = 3.3V	1.2	1.9	V
V_{OL}	Static output low level			0.3	V
V_{OH}	Static output high level		2.8	3.6	V
V_{HSSQ}	High-speed suppression information detection threshold		100	150	mV
V_{HSDSC}	High-speed disconnection detection threshold		500	625	mV
V_{HSOI}	High-speed idle level		-10	10	mV
V_{HSOH}	High-speed data high level		360	440	mV
V_{HSOL}	High-speed data low level		-10	10	mV

4.3.16 12-bit ADC characteristics

Table 4-27 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.4		3.6	V
V_{REF+}	Positive reference voltage	V_{REF+} cannot be more than V_{DDA}	2.4		V_{DDA}	V
I_{VREF}	Reference current			160	220	uA
I_{DDA}	Supply current			480	530	uA
f_{ADC}	ADC clock frequency				14	MHz
f_S	Sampling rate		0.05		1	MHz
f_{TRIG}	External trigger frequency				16	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0		V_{REF+}	V
R_{AIN}	External input impedance				50	kΩ
R_{ADC}	Sampling switch resistance			0.6	1	kΩ

C_{ADC}	Internal sample and hold capacitor			8		pF
t_{CAL}	Calibration time	Other		40		$1/f_{ADC}$
t_{lat}	Injected trigger conversion latency				2	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency				2	$1/f_{ADC}$
t_s	Sampling time		1.5		239.5	$1/f_{ADC}$
t_{STAB}	Power-on time				1	us
t_{CONV}	Total conversion time (including sampling time)		14		252	$1/f_{ADC}$

Note: Above parameters are guaranteed by design.

Formula: Maximum R_{AIN}

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 4-28 Maximum RAIN when f_{ADC} = 14MHz

T_S(cycle)	t_S (us)	Maximum R_{AIN}(kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	Invalid
239.5	17.1	Invalid

Table 4-29 ADC error

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
EO	Offset error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3.3V		±2		LSB
ED	Differential nonlinearity error			±0.5	±3	
EL	Integral nonlinearity error			±1	±4	

C_p represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger C_p value will reduce the conversion accuracy, the solution is to reduce the f_{ADC} value.

Figure 4-12 ADC typical connection diagram

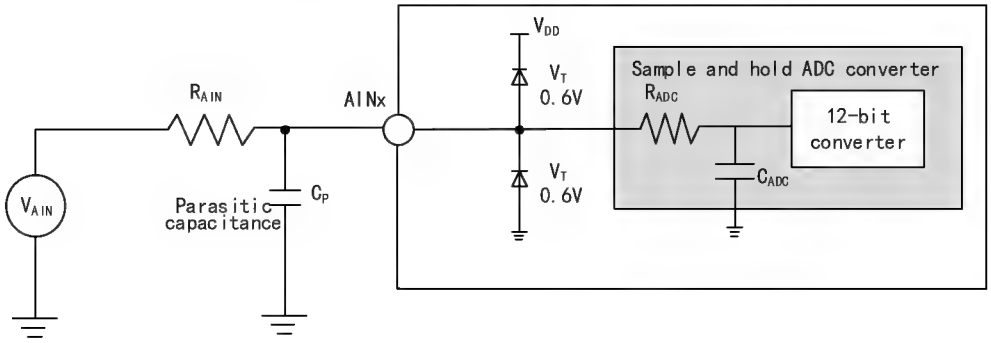
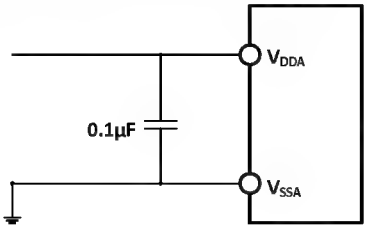


Figure 4-13 Analog power supply and decoupling circuit reference



4.3.17 Temperature sensor characteristics

Table 4-30 Temperature sensor characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_{TS}	Measurement range of temperature sensor		-40		85	℃
A_{TSC}	Measurement range of temperature sensor after software calibration			±12		℃
Avg_Slope	Average slope (negative temperature coefficient)		3.8	4.3	4.8	mV/℃
V_{25}	Voltage at 25℃		1.34	1.40	1.46	V
T_{S_temp}	ADC sampling time when reading temperature	f_{ADC} = 14MHz			17.1	us

4.3.18 OPA characteristics

Table 4-31 OPA characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.4	3.3	3.6	V
C_{MIR}	Common mode input voltage		0		V_{DDA}-0.9	V
$V_{IOFFSET}$	Input offset voltage			2.5	8	mV
I_{LOAD}	Drive current				600	uA
$I_{DDOPAMP}$	Current consumption	No load, static mode		195		uA
C_{MRR}(1)	Common mode rejection ratio	@1KHz		96		dB
P_{SRR}(1)	Power supply rejection ratio	@1KHz		86		dB

A_V(1)	Open loop gain	C_{LOAD}=5pF		136		dB
G_{BW}(1)	Unit gain bandwidth	C_{LOAD}=5pF		19		MHz
P_M(1)	Phase margin	C_{LOAD}=5pF		93		
S_R(1)	Slew rate limited	C_{LOAD}=5pF		8		V/us
t_{WAKUP}(1)	Setup time from shutdown to wake up, 0.1%	Input $V_{DDA}/2$, C_{LOAD}=5pF,R_{LOAD}=4kΩ			368	ns
R_{LOAD}	Resistive load		4			kΩ
C_{LOAD}	Capacitive load				50	pF
V_{OHSAT}(2)	High saturation output voltage	R_{LOAD}=4kΩ, input V_{DDA}	V_{DDA}-45			mV
		R_{LOAD}=20kΩ, input V_{DDA}	V_{DDA}-10			
V_{OLSAT}(2)	Low saturation output voltage	R_{LOAD}=4kΩ, input 0			0.5	mV
		R_{LOAD}=20kΩ, input 0			0.5	
EN(1)	Equivalent input voltage noise	R_{LOAD}=4kΩ,@1KHz		83		$\frac{nv}{\sqrt{Hz}}$
		R_{LOAD}=4kΩ,@10KHz		42		

Note: 1. Design parameters are guaranteed.

2. The load current limits the saturated output voltage.

Chapter 5 Package and ordering information

Packages

Part No.	Package	Body size	Lead pitch	Description	Packing type
CH32F208RBT6	LQFP64M	10*10mm	0.5mm	LQFP64M (10*10) patch	Tray
CH32F208WBU6	QFN68X8	8*8mm	0.4mm	Quad no-lead 68-pin	Tray

Note: 1. The packing type of QFP/QFN is usually tray. Please confirm with the packaging factory for specific part number.

*2. Size of tray: The size of tray is generally a uniform size (322.6*135.9*7.62). There are differences in the size of the restriction holes for different package types, and there are differences between different packaging factories for tubes, please confirm with the manufacturer for details.*

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or 10%.

Figure 5-1 QFN68X8 package

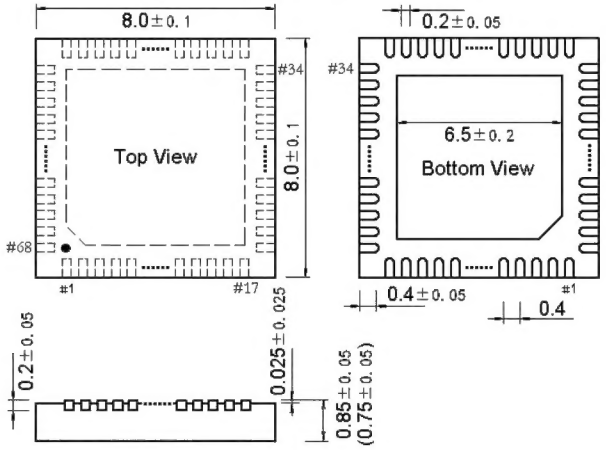
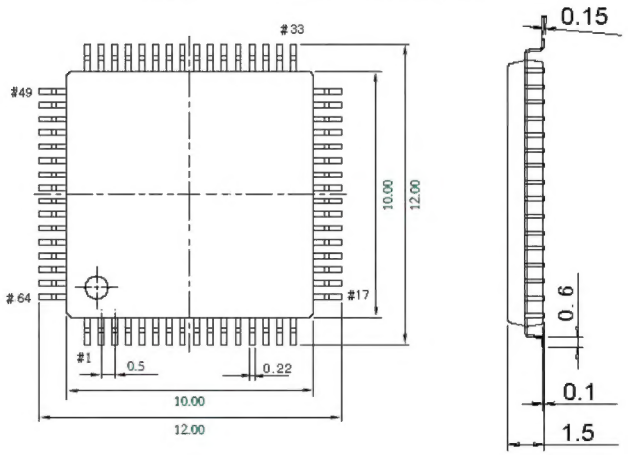


Figure 5-2 LQFP64M package



Series product naming rules

Example: CH32 V 3 03 R 8 T 6

Device family

F = ARM-based

V = QingKe RISC-V-based

Product type

0 = QingKe V2 core

1 = M3/ QingKe V3A core, clock speed @72M

2 = M3/ QingKe V4B_C core, clock speed @144M

3 = QingKe V4F floating-point core, clock speed @144M

Device subfamily

03 = General-purpose

05 = Connectivity (USB high-speed, SDIO, dual CAN)

07 = Interconnectivity (USB high-speed, dual CAN, Ethernet, DVP, SDIO, FSMC)

08 = Wireless (BLE5.3, CAN, USB, Ethernet)

Pin count

J = 8 pins	A = 16 pins	F = 20 pins
G = 28 pins	K = 32 pins	T = 36 pins
C = 48 pins	R = 64 pins	W = 68 pins
V = 100 pins	Z = 144 pins	

Flash memory size

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

Package

T = LQFP

U = QFN R = QSOP

P = TSSOP M = SOP

Temperature range

6 = -40°C～85°C (industrial-grade)

7 = -40°C～105°C (automotive-grade 2)

3 = -40°C～125°C (automotive-grade 1)

D = -40°C～150°C (automotive-grade 0)